1. Amendments to the Claims:

A listing of the entire set of pending claims (including amendments to the claims, if any) is submitted herewith per 37 CFR 1.121. This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) Data processing system comprising:

- a clustered Instruction Level Parallelism processor, comprising a plurality of clusters each comprising at least one register file and at least one functional unit;
- an instruction unit for issuing control signals to said clusters,

wherein said instruction unit is connected to each of said clusters via respective control connections, and

one or more additional pipeline registers is arranged in said control connections depending on the distance between said instruction unit and said clusters,

and wherein said pipeline registers **are between any two of said clusters with** ~~being adapted to provide~~ a dedicated direct signal data signal connection **there**between ~~any two of said clusters~~.

2. (Previously Presented) Data processing system according to claim 1, wherein said clusters are connected to each other via a point-to-point connection.

3. (Previously Presented) Data processing system according to claim 1, wherein said clusters are connected to each other via a bus connection.

4. (Previously Presented) Data processing system according to claim 3, wherein said control connections are implemented as a bus.

5. (Currently Amended) A clustered Instruction Level Parallelism processor, comprising:

- a plurality of clusters each comprising at least one register file and at least one functional unit;
- an instruction unit for issuing control signals to said clusters,

wherein said instruction unit is connected to each of said clusters via respective control connections, and

one or more additional pipeline registers are arranged in said control connections depending on the distance between said instruction unit and clusters,

and wherein said pipeline registers **are between any two of said clusters with** ~~being adapted to provide~~ a dedicated direct signal data signal connection **there**between ~~any two of said clusters~~.

6. (Previously Presented) The clustered Instruction Level Parallelism processor as claimed in claim 5, wherein said clusters are connected to each other via a point-to-point connection.

7. (Previously Presented) The clustered Instruction Level Parallelism processor as claimed in claim 5, wherein said clusters are connected to each other via a bus connection.

8. (Previously Presented) The clustered Instruction Level Parallelism processor as claimed in claim 7, wherein said control connections are implemented as a bus.